



Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No. NOVLP068/NVLS-2818 Applicant: Koos et al. Filing Date October 20, 2003	Application No.: 10/690,084 Group 1765
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U.S. Patent and Publication Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
LV	A1	4,002,778	1/11/77	Bellis et al.			
	A2	6,692,873	11/8/05	Park			
	A3	5,824,599	10/20/98	Schacham-Diamond, et al.			
	A4	5,695,810	12/9/97	Dubin et al.			
	A5	5,380,560	1/10/945	Kaja et al.			
	A6	6,197,364	3/6/01	Paunovic et al.			
	A7	2002/0084529	07/2002	Dubin et al.			
LV	A8	2003/0176049	09/2003	Hegde et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
LV	B1	JP03122266	05/1991	JPO				

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
LV	C1	Sullivan et al, "Electrolessly Deposited Diffusion Barriers For Microelectronics, E. J. IBM J Res Develop Vol 42, No. 4 Sept 1998, 607-620
LV	C2	Eugene J. O'Sullivan, "Electroless Deposition in Microelectronics: New Trend," Electrochemical Society Proceeding Volume 99-34, 159-171
LV	C3	T. Itabashi et al., "Electroless Deposited CoWB for Copper Diffusion Barrier Metals," Hitachi Research Laboratory, IEEE, 2002, 285-287
LV	C4	N. Petrov and Y. Shacham-Diamand, "Electrochemical Study of the Electroless Deposition of Co(W,P) Barrier Layers for Cu Metallization," Electrochemical Soc. Proceedings Vol. 2000-27, 134-148
Examiner /Lan Vinh/		Date Considered 11/22/2006

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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LV	C5	Yosi Shacham-Diamand and Sergey Lopatin, "Integrated Electroless Metallization for ULSI," Electrochimica Acta, (44 (19999) 3639-3649
LV	C6	Theoretical Studies on the Electroless Metal Deposition Reaction Mechanism Group, printed from website http://www.appchem.waseda.ac.jp on 7/3/02. Published prior to the filing of this application. 3 Pages
LV	C7	Wolf, Silicon Processing for the VLSI Era, Lattice Press, Vol. 3, Page 648
Examiner /Lan Vinh/		Date Considered 11/22/2006

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